(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 334 627 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **89302830.8**

(51) Int. Cl.[5]: **G06F 15/16**

(22) Date of filing: **22.03.89**

(30) Priority: **23.03.88 GB 8806849**
23.03.88 GB 8806851
23.03.88 GB 8806852
23.03.88 GB 8806859
23.03.88 GB 8806860
23.03.88 GB 8806871

(43) Date of publication of application:
27.09.89 Bulletin 89/39

(84) Designated Contracting States:
DE FR GB IT NL

(88) Date of deferred publication of the search report:
12.06.91 Bulletin 91/24

(71) Applicant: **DU PONT PIXEL SYSTEMS LIMITED**
Wedgewood Way
Stevenage Hertfordshire SG1 4QN(GB)

(72) Inventor: **Baldwin, David Robert**
Hanover Cottage 22 Dresden Way
Weybridge Surrey, KT13 9AU(GB)
Inventor: **Kent, Osman**
Knavesmire St Leonard's Road
Thames Ditton Surrey(GB)
Inventor: **Ahishalilar, Yavuz**
Highlands Warren Park Coombe Hill
Kingston-upon-Thames Surrey, KT2 7HX(GB)

(74) Representative: **Targett, Kenneth Stanley et al**
D. Young & Co. 10 Staple Inn
London WC1V 7RD(GB)

(54) Multiprocessor architecture.

(57) A numeric processing subsystem, where at least three processors concurrently run separate processes. One of the three is a control processor (110), one is a data transfer processor (120), which controls the external interface, and one or several are numeric processors (130). Preferably this subsystem also includes at least a megabyte of cache memory (140), which is linked to the floating-point processor by a very high-bandwidth bus.

The interface to the numeric processor(s) is so constrained that a variety of integrated circuits can be readily substituted. To compensate for the different pin-out and routing requirements of different chips, exchangeable subboards are preferably used to mount the arithmetic chips. To achieve this chip-independence without sacrificing speed, an extremely flexible and highly multiported register file is used at the interface from the cache memory (140) to the numeric processing subsystem. To achieve algorithm flexibility, parallel writes from data cache memory to the control storage of the numeric processing subsystem are preferably possible.

At least one of the numeric processors is preferably a floating-point processors, and one or more others may be application-customized processors. The application-customized processor is especially well adapted for some particular class of operations, such as discrete Fourier transform operations, and the numeric processor provides acceptably high speed on the general range of numeric computations.

The data transfer processor (120) controls several external interfaces, including a port, for configuring multiple subsystems together, which includes two high-bandwidth input ports and a high-bandwidth output port. This permits a wide variety of highly pipelined and/or parallel architectures to be readily implemented.

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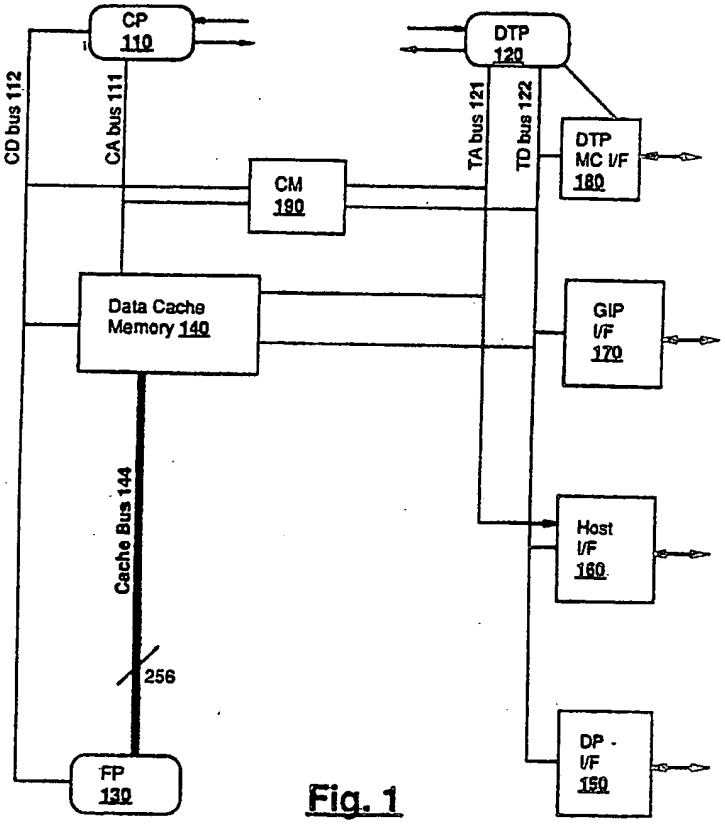

CP
110
DTP
120
CD bus 112
CA bus 111
TA bus 121
TD bus 122
DTP
MC I/F
180
CM
190
Data Cache
Memory 140
GIP
I/F
170
Cache Bus 144
Host
I/F
160
256
DP -
I/F
150
FP
130

Fig. 1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 30 2830

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	BUREAUX D'ETUDES AUTOMATISMES, no. 32, mars 1987, pages 85-87; J. GUSTAFSON: "Un super-ordinateur vectoriel homogène" * Page 85, figure; page 85, left-hand column, line 35 - page 87, middle column, line 9 *	11,12	G 06 F 15/16 G 06 F 15/06
A	IDEM	13,18,20	
A	US-A-4 722 049 (LAHTI) * Figures 1,4,8,9,12; column 2, line 60 - column 4, line 28; column 22, line 42 - column 23, line 53 *	1-10	
A	US-A-4 172 287 (KAWABE) * Figure 3; column 1, line 47 - column 2, line 2 *	1	
A	EP-A-0 085 435 (HITACHI) * Figure 3; page 6, line 15 - page 9, line 6 *	1	
A	WO-A-8 607 174 (SHEKELS) * Figure 2; page 12, line 3 - page 14, line 2 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
G 06 F 15

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	04 March 91	SCHENKELS P.F.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
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D: document cited in the application
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